CLAIMS

1. A circuit coupled to an output device, the circuit comprising at least one transistor device adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress.

2. The circuit of Claim 1, further comprising two stacked transistor devices coupled to the output device.

3. The circuit of Claim 1, wherein said transistor device comprises at least one p-channel transistor coupled to the output device.

4. The circuit of Claim 1, wherein said transistor device comprises two stacked p-channel transistors coupled to the output device.

5. The circuit of Claim 1, wherein the output device comprises at least one n-channel output transistor.

6. The circuit of Claim 1, wherein the output device comprises two stacked n-channel transistors.

7. An integrated circuit comprising:

an output circuit; and

a stress circuit coupled to at least said output circuit and adapted to limit a duration of a high voltage across said output circuit thereby reducing hot carrier injection stress.

8. The integrated circuit of Claim 7, wherein said stress circuit comprises stacked transistors.

9. An integrated circuit comprising:

an IO PAD;

an output circuit coupled to at least said IO PAD; and

a stress circuit coupled to at least said output circuit and adapted to limit a duration of a high voltage across said output circuit when said output circuit is enabled, thereby reducing stress on said output circuit.

10. The integrated circuit of Claim 9, wherein said stress circuit comprises at least one transistor.

11. The integrated circuit of Claim 10, wherein said transistor comprises at least one p-channel transistor.

12. The integrated circuit of Claim 10, wherein said transistor comprises two stacked p-channel transistors.

13. The integrated circuit of Claim 9, wherein said output circuit comprises at least one transistor.

14. The integrated circuit of Claim 13, wherein said transistor comprises an n-channel transistor.

15. The integrated circuit of Claim 13, wherein said transistor comprises two stacked n-channel transistors.

16. The method of controlling hot carrier injection stress comprising limiting a duration of a high voltage across an output device.

17. The method of Claim 16, further comprising using a stress circuit to limit said duration of said high voltage across said output device when said output device is enabled.

18. A method of reducing stress across an output circuit, comprising:

determining if the output circuit is tri-stated;

determining if a PAD voltage is greater than a predetermined voltage level;

enabling the output circuit;

turning on a stress circuit, dissipating a voltage across the output circuit; and

preventing the output circuit from experiencing HCI stress.

19. A method of reducing hot carrier injection stress in an integrated circuit comprising:

enabling an output device in the integrated circuit; and

limiting a duration of a high voltage across said output device.

20. The method of Claim 19, further comprising determining if a voltage on an IO PAD is greater than an IO power supply voltage.

21. The method of Claim 19, further comprising turning on at least one n-channel transistor of said output device.